Digital I/O Connections

Safely connect external hardware to 68HC11 digital I/O pins without damage.

On the QCard Controller the 68HC11 processor's port A is available for you to connect to external devices. You can use processor pins to directly drive LEDs, relays, transistors, opto-isolators or other digital logic devices. But please be careful – whenever these outputs are connected to external devices you must stay within the voltage and current capabilities of the output pins. Because the MC68HC11 reference manuals don't specify the electrical capability of these ports very well we provide some additional information here.

Electrical characteristics of the 68HC11's I/O ports

The electrical characteristics of the Freescale 68HC11F1 processor's digital I/O signals are specified in detail on page A-3 of the   MC68HC11F1 Technical Data Manual. A table there lists the "DC Electrical Characteristics" of the processor.

Input pin logic levels

Pins on the 68HC11 configured as digital inputs report a logical *high* if the input voltage is greater than 0.7 times the supply voltage, or 3.5 Volts. They report a logical *low* if the input voltage is less than 0.2 times the supply voltage, or 1.0 Volt. Input voltages between 1.0 and 3.5 Volts are not guaranteed to be consistently read as either high or low.

Output pin logic levels

Pins on the 68HC11 configured as digital outputs in the *high* state can maintain the output voltage within 0.8 Volts of the positive supply if 0.8 mA or less is drawn from the pin. If less than 10 microamps is drawn, the output high voltage is within 0.1 Volt of the positive supply. In the *low* state, the digital outputs can keep the voltage below 0.4 Volts while sinking up to 1.6 mA of current. Load circuitry that requires significant current to be sourced or sunk by the digital output should include external resistors to ensure that the absolute maximum rating of 25 mA per output pin is never exceeded.

Output pin V-I (Voltage-Current) characteristics

The output pins of the MC68HC11 are similar in electrical characteristics to the SN54/74HC digital logic family. They can source or sink up to 25 mA and are guaranteed to source 0.8 mA while providing a valid logic high and to sink 1.6 mA at a valid logic low, although they generally do much better.

A valid logic high level is between $V_{OH} = V_{DD}$ and $V_{OH} = V_{DD} - 0.8$ V, and a valid low level is between $V_{OL} = V_{SS} = 0$ V and $V_{OL} = V_{SS} + 0.4$ V. It is often useful to know just how much to expect the V_{OL} and V_{OH} levels to degrade with current. As the output is loaded, the V_{OL} and V_{OH} levels rise or fall, the amount depending on the current sourced or sunk. For currents of less than

10 mA the voltage change is linear with current; that is, it can be modeled as a voltage source of either zero or five volts and an equivalent series resistance of 40 ohms. At greater output currents the resistance increases until at the greatest specified current for any one pin, 25 ma., the equivalent resistance is 60 ohms. At this current the voltage degradation of the V_{OL} or V_{OH} is 1.5 volts. The following two graphs illustrate this variation.

These graphs can be used to choose component values for particular circuits. For example if we wish to use a pin of Port A to drive a light-emitting diode we would place the LED in series with a resistor and connect them between an output pin and ground. The resistor limits the current, to the LED. From the LED data sheet we note that its forward voltage at a current of 10 mA is specified to be 2.2 V. What should the resistor value be? We calculate it as,
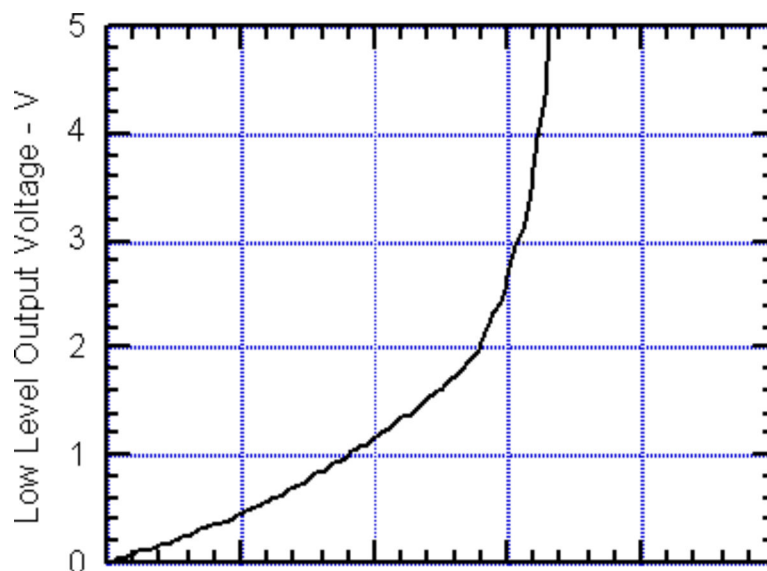
$$R = (V_{OH} - 2.2 \text{ V}) / 10 \text{ mA} \qquad\qquad\qquad \textbf{Eqn. 1}$$

Consulting the V_{OH} vs I curve for the output pin we find that at 10 mA V_{OH} = 4.4 V. We therefore need a resistance of 220 ohms.
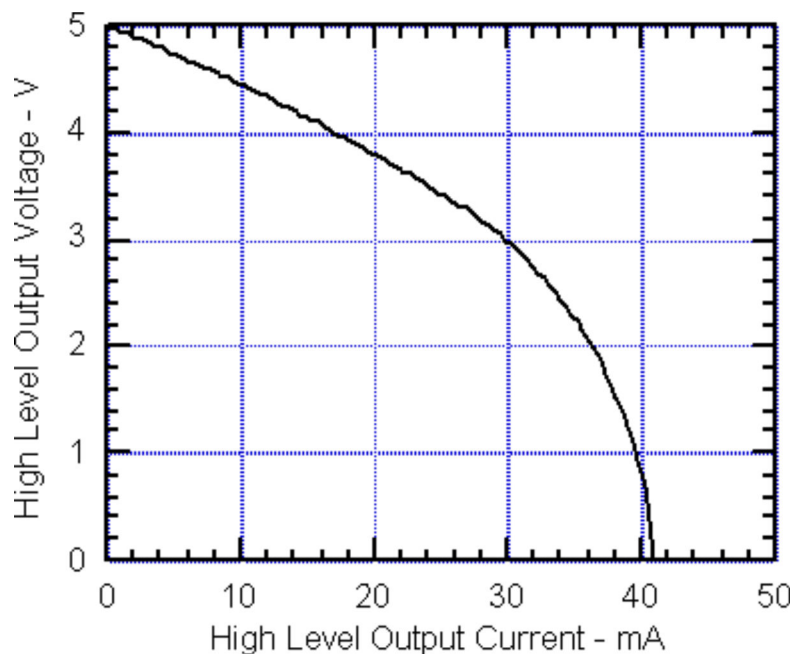
Degradation of the Port A or Port D output high voltage with current. The maximum current allowed for continuous operation is 25 ma.

| 0   10   20   30   40   50 |

Low Level Output Current - mA

**Degradation of the Port A or Port D output low voltage with current. The
maximum current allowed for continuous operation is 25 ma.**

Protecting the input and output pins

These output pins are very useful because they can directly drive a wide range of devices.
Nevertheless, any circuitry connected to the processor should take care to:

   1. Prevent excessive voltage levels at the pin; and,

   2. Prevent excessively great currents.

We'll address each of these concerns in turn.

Preventing excessive voltages on IO pins

Excessive voltages are prevented by ensuring that voltages of less than a diode drop below V_{SS}
(-0.6 V) or greater than a diode drop above V_{DD} (V_{DD}+0.6 V) are never applied to the processor.
For some applications, particularly when driving inductive loads such as relays, you may need to
provide Schottkey diode clamps between the pin and V_{DD} and between the pin and ground.

All pins on the processor have inherent diode clamps to the processor's ground voltage, V_{SS}, but it
is best not to rely on these; if there is the possibility of the output pin being driven to a negative
voltage level it is better to prevent excessive power dissipation in the processor package by
externally clamping the voltage to ground (V_{SS}) with a Schottkey diode. Processor port A pins also
have inherent diode clamps to the chip's +5V supply voltage, V_{DD}, but it is better not to rely on
these; instead external Schottkey clamps to V_{DD} should be used.

Preventing excessive currents

The current into or out of any pin on the MC68HC11 should also be limited to prevent damage.
The specified maximum current is 25 mA into or out of any one pin at a time, although these pins
can typically withstand transients of more than 100 mA at room temperature. In driving more than
one pin at a time it is necessary only to stay within the processor's maximum power dissipation.
Unfortunately, Motorola doesn't specify what this maximum is, but we recommend that you don't
exceed a total of 100 mW for all processor I/O pins combined. The chip's total power dissipation
is the sum of its internal power (which varies from device to device so much that it can only be
determined by actually measuring it, but which is specified at less than 150 mW) and the power
associated with the I/O pins. Pin currents must be limited using external resistors.